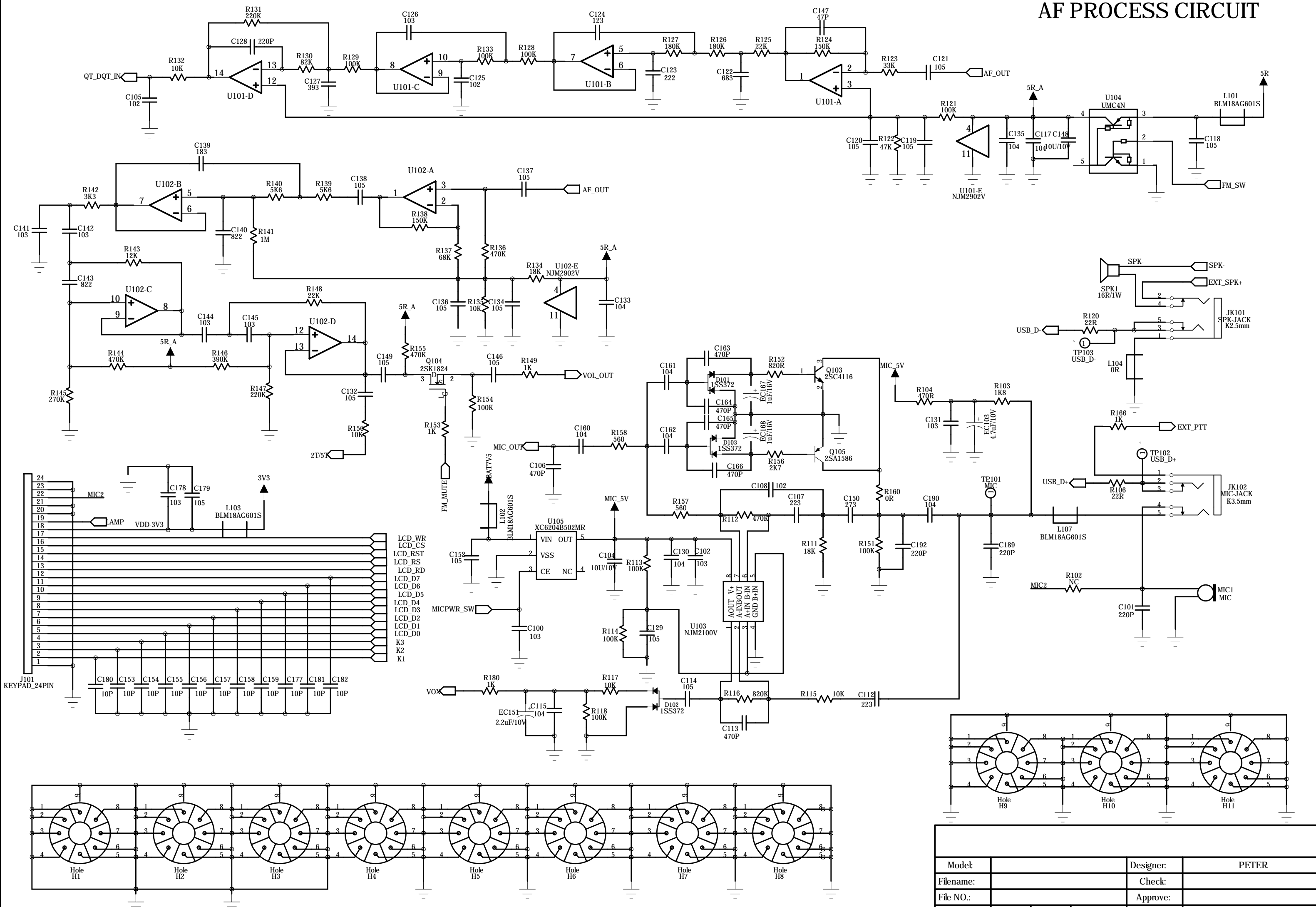
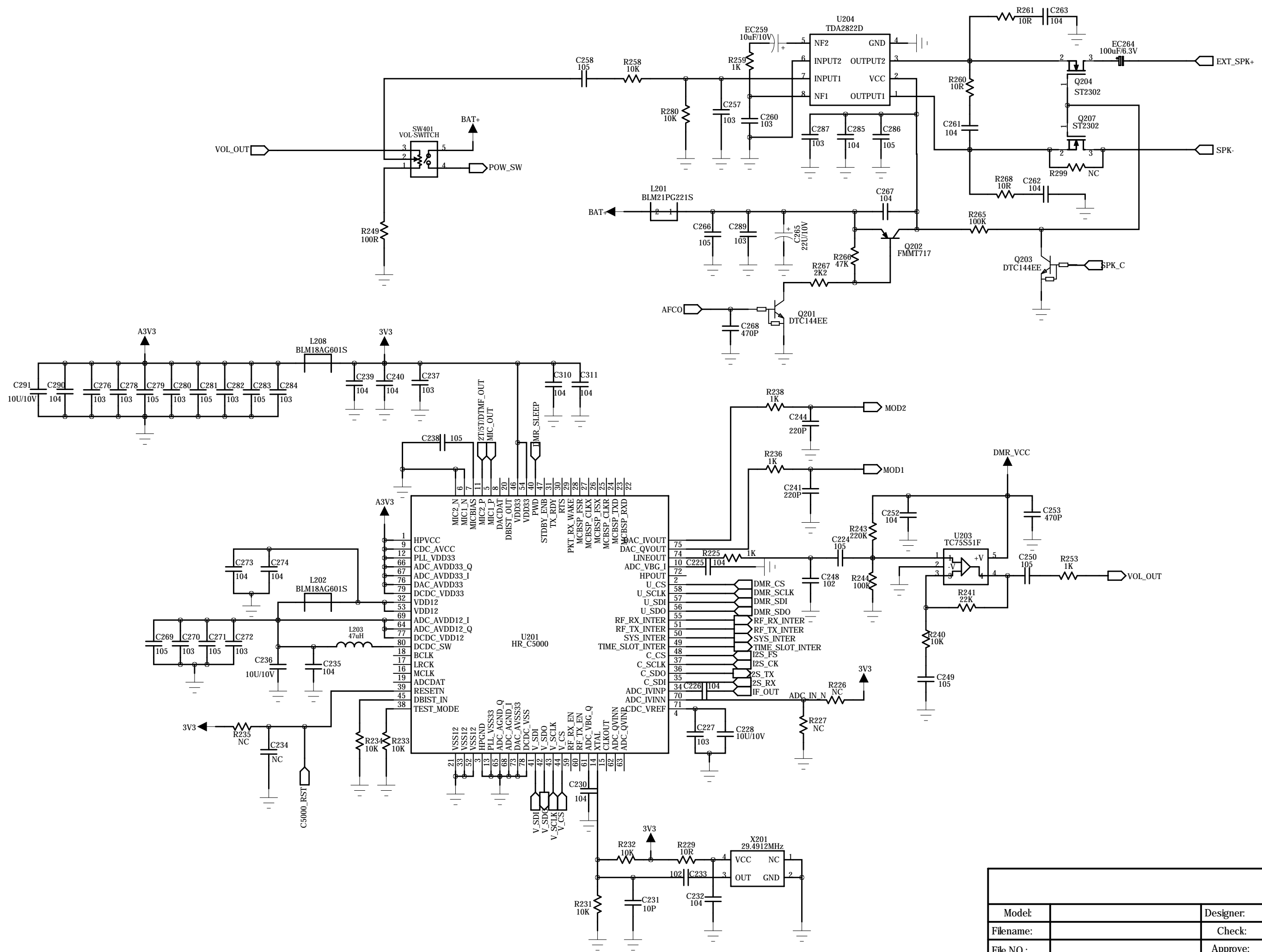


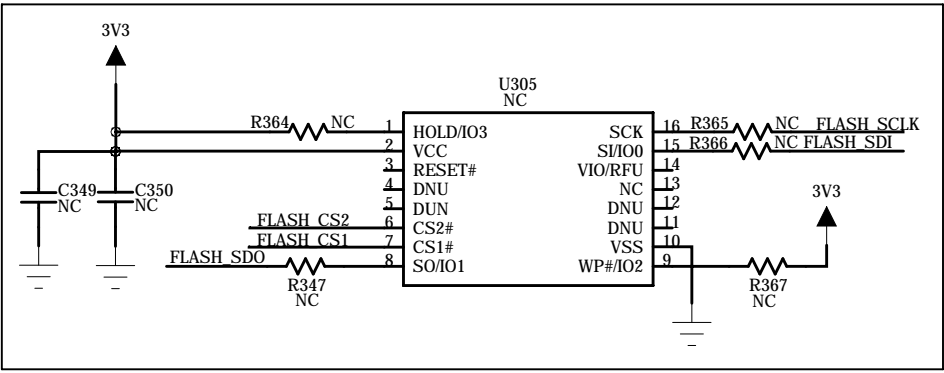
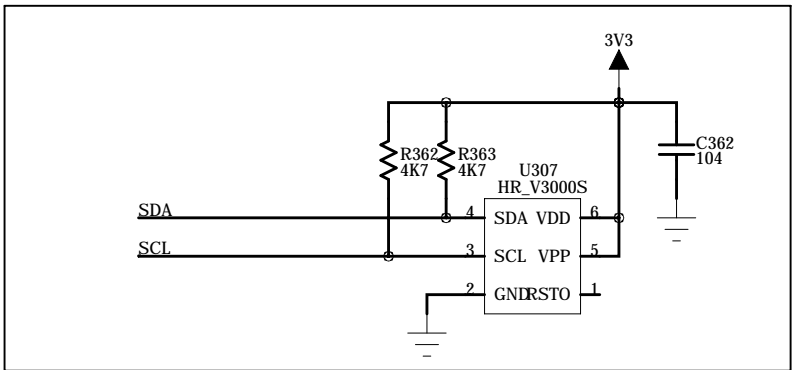
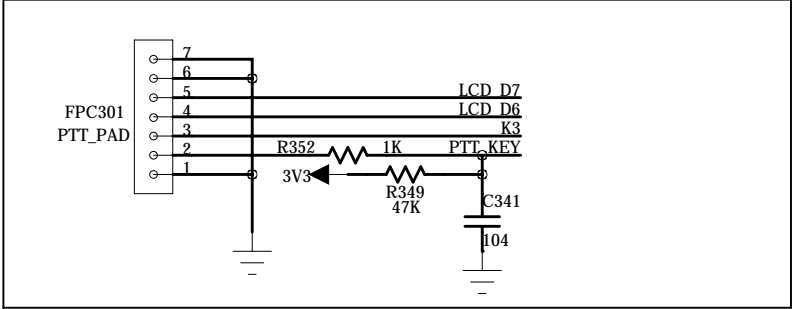
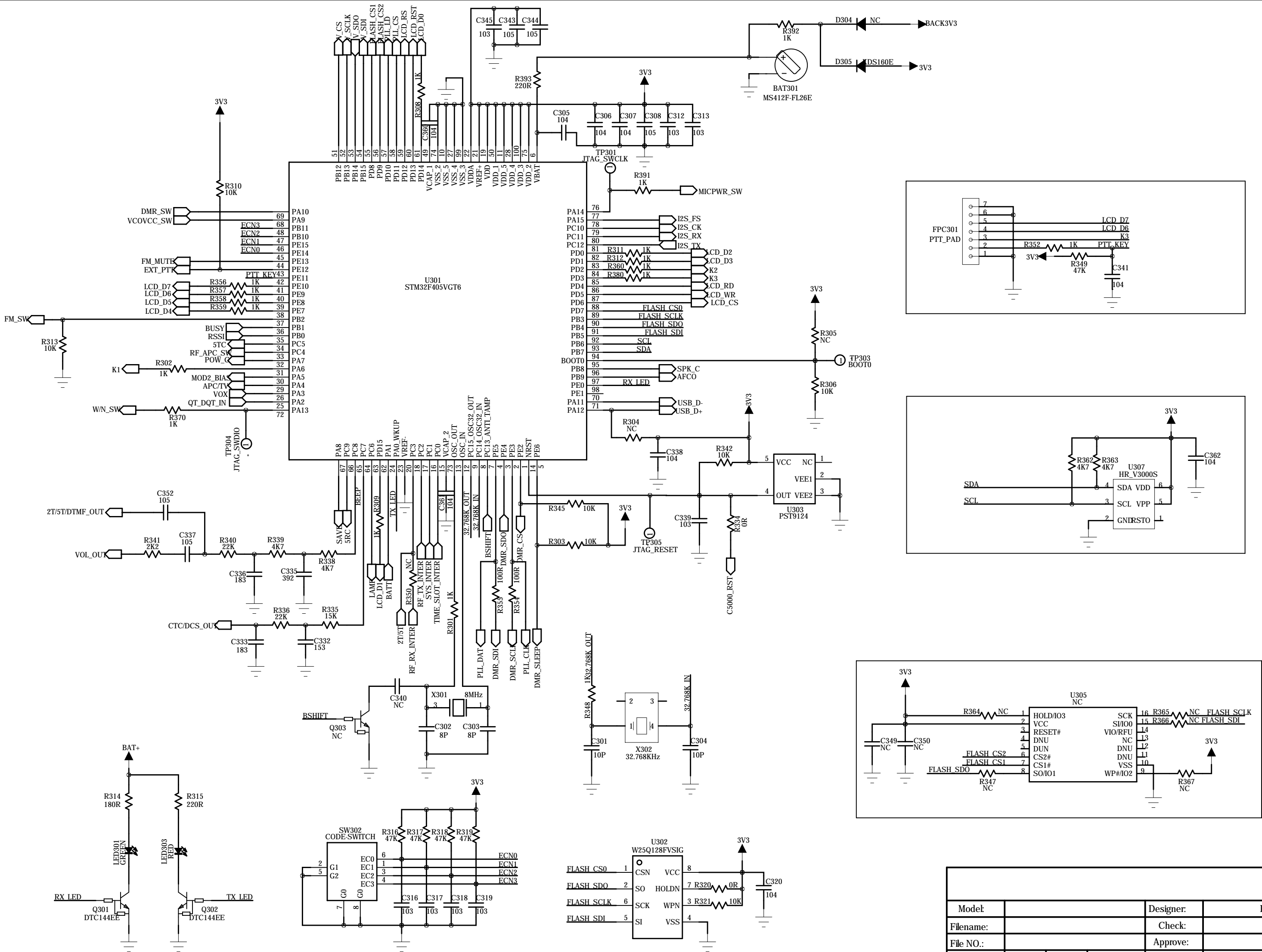
AF PROCESS CIRCUIT



Model:		Designer:	PETER		
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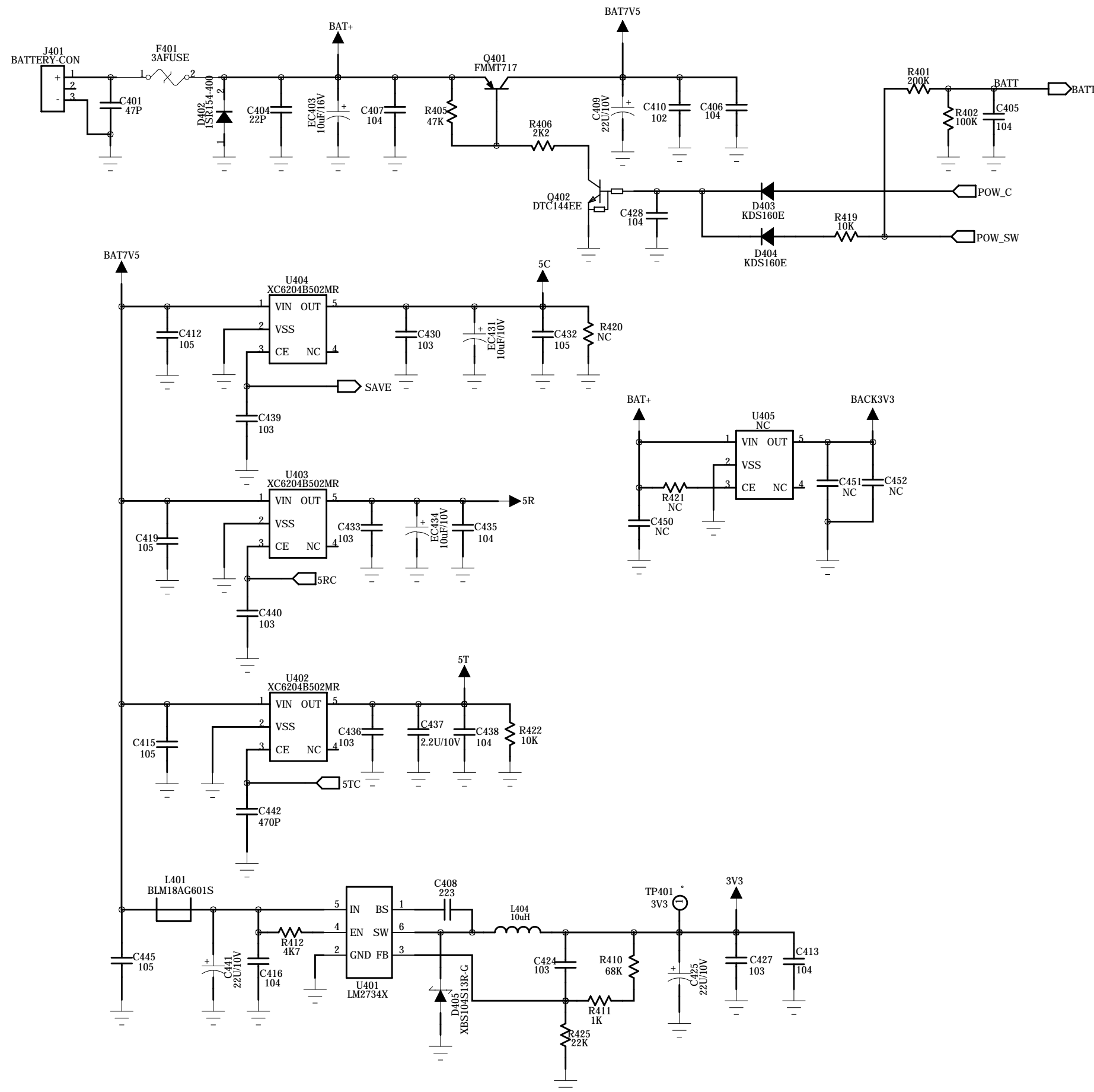


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		DATE:	2014.08.11



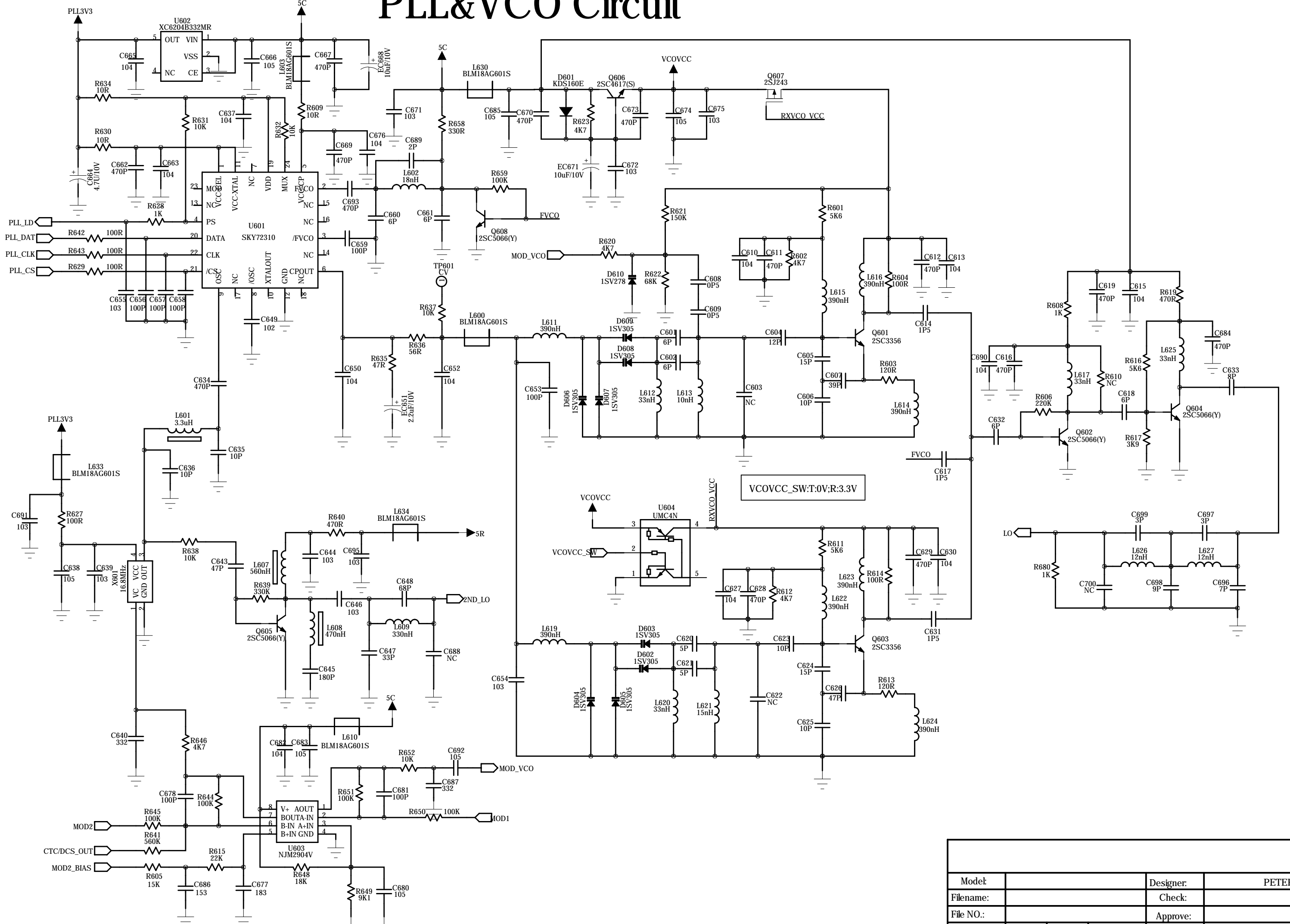
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REV:	1.0	Page:	3 of 6	DATE:	2014.08.11

POWER CIRCUIT



Model:		Designer:	PETER		
Filename:		Check:			
File NO.:		Approve:			
REV:	1.0	Page:	4 of 6	DATE:	2014.08.11

PLL&VCO Circuit



Model:		Designer:	PETER		
Filename:		Check:			
File NO.:		Approve:			
REV:	1.0	Page:	6 of 6	DATE:	2014.08.11